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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/607,680	06/30/2000	Brad A. Barmore	042390.P8527	1233

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EXAMINER	
CASIANO, ANGEL L	
ART UNIT	**PAPER NUMBER**
2182	10

DATE MAILED: 11/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/607,680	BARMORE, BRAD A.	
	Examiner	Art Unit	
	Angel L. Casiano	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is in response to amendment filed 05 August 2003.

2. Claims 1-27 are pending.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05 August 2003 has been entered.

Drawings

4. Objection to the Drawings has been overcome with corrections filed in the Amendment.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-2, 4-11, 13-20, and 22-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pecone [US 5,604,871] in view of Chang et al. [US 2001/0014927 A1].

Regarding Claim 1, Pecone discloses a system including a motherboard (col. 2, lines 49-50) coupled to data, address, control, power and ground signals, as well as a riser card having interface and logic circuits (col. 2, lines 53-54). Although the reference does not explicitly mention a chipset, it would have been obvious to one of ordinary skill in the art that the term "chipset" referred to integrated circuits designed to perform one or more functions. The reference also discloses a memory, intended to store a sequence of instructions, coupled with the motherboard (col. 3, lines 33-35). Accordingly, Pecone also teaches a riser card coupled with the motherboard (col. 7, lines 1-4; lines 34-38), having a circuit (col. 4, line 67; col. 5, lines 2-5; col. 3, line 35) that interacts with a portion of the integrated circuits ("chipset") to provide a functionality (col. 3, line 37) and having a memory (col. 3, line 34) to store one or more indications of the functionality. Pecone does not include a sequence of instructions to cause a driver to be loaded based, at least in part, on the one or more indications. In addition, Pecone does not expressly disclose the riser card operating as a logical extension of the motherboard. Furthermore, Pecone fails to provide an external interface for the motherboard. Chang et al. teaches a riser card operating as an extension of the motherboard (see Figs. 1-4, "30", "38"; [0023], [0024], [0028]). The riser card (see "30"), as presented by Chang et al. provides an external interface for the motherboard (see [0034]). Chang et al. does not explicitly cite causing a driver to be loaded. However, it does teach a riser card having "plug-in"

functionality (see [0001]). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention to cause a driver to be loaded in order to provide plug and play (PnP) functionality. Moreover, it is well known in the art that a "driver" refers to code that works to communicate an operating system and a peripheral. Being a plug-in riser card part of the hardware, it would have been obvious to include a driver that would specifically load the required code in order to make the claimed system functional. Furthermore, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to obtain a system having integrated functionality at a low cost (see Chang et al., [0004], [0012], [0013]).

As for Claim 2, the Pecone reference includes a riser card coupled with the motherboard via a slot interface having pins (see col. 8, lines 13-17; col. 7, lines 34-38) corresponding to one or more predetermined standards (see col. 3, lines1-3).

As for Claims 4-8, the claimed functionalities constitute specific examples of the possible applications of the system disclosed by the combination of references and exposed in claim 1. Therefore, these claims are rejected under the same rationale.

As for Claim 9, Pecone fails to include a sequence of instructions to cause a driver to be loaded. Chang et al. does not explicitly cite causing a driver to be loaded. However, it does teach a riser card having "plug-in" functionality (see [0001]). Accordingly, it would

have been obvious to one of ordinary skill in the art at the time of the invention to cause a driver to be loaded in order to provide plug and play (PnP) functionality.

Regarding Claim 10, Pecone teaches a system including a motherboard (col. 2, lines 49-50) and a riser card having an interface and logic circuits (col. 2, lines 53-54). Although the reference does not explicitly mention a coupled "chipset", it would have been obvious to one of ordinary skill in the art that the term "chipset" implied integrated circuits designed to perform one or more functions. This term is commonly used in reference to the core functionality of a motherboard. The reference discloses a memory, intended to store a sequence of instructions, coupled with the motherboard (col. 3, lines 33-35). In addition, Pecone teaches a riser card coupled with a motherboard (col. 7, lines 1-4; lines 34-38), having a circuit (col. 4, line 67; col. 5, lines 2-5; col. 3, line 35) that interacts with a portion of the integrated circuits (see "chipset") to provide a functionality (col. 3, line 37) and also having a memory (col. 3, line 32) to store one or more indications of the functionality. Pecone does not include a sequence of instructions to cause a driver to be loaded based, at least in part, on the one or more indications. Chang et al. teaches a riser card operating as an extension of the motherboard (see Figs. 1-4, "30", "38"; [0023], [0024], [0028]). The riser card (see "30"), as presented by Chang et al. provides an external interface for the motherboard (see [0034]). Chang et al. does not explicitly cite causing a driver to be loaded. However, it does teach a riser card having "plug-in" functionality (see [0001]). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention to cause a driver to be loaded in order to

provide plug and play (PnP) functionality. It is well known in the art that a driver is a code that works to communicate an operating system and a peripheral. It would have been obvious to one of ordinary skill in the art, since a plug-in riser card is hardware, to include a driver that specifically loads the required code in order to make the claimed riser card functional. Furthermore, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to obtain a system having integrated functionality at a low cost (see Chang et al., [0004], [0012], [0013]).

As for Claim 11, the reference teaches a riser card coupled with the motherboard via a slot interface having pins corresponding to one or more predetermined standards (see col. 8, lines 13-17; col. 7, lines 34-38; col. 3, lines 1-3; col. 5, lines 6-7).

As for Claims 13-17, these limitations (audio codec, modem codec, USB support, SMBus device support, and networking functionality) constitute specific examples of the possible applications for the riser card disclosed by the combination of references, as exposed previously. Therefore, these claims are rejected under the same rationale.

As for Claim 18, Pecone does not explicitly disclose a sequence of instructions to cause a driver to be loaded based, at least in part, on the one or more indications. Chang et al. does not explicitly cite causing a driver to be loaded. However, it does teach a riser card having "plug-in" functionality (see [0001]). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention to cause a driver to be loaded in

order to provide plug and play (PnP) functionality. A driver is code that works to communicate an operating system and a peripheral. Thus, it would have been obvious to someone of ordinary skill in the art to include a driver that would specifically load the required code in order to make the plug-in riser card functional.

Regarding Claim 19, the reference discloses a memory, for storing a sequence of instructions, coupled with the motherboard (col. 3, lines 33-35), as claimed. The reference also discloses a system comprising a motherboard (col. 2, lines 49-50) coupled to data, address, control, power and ground signals, as well as a riser card having an interface and logic circuits (col. 2, lines 53-54). Although the reference does not explicitly mention a "chipset", as it is well known in the art, the term "chipset" refers to integrated circuits designed to perform one or more functions. This term is commonly used in reference to the core functionality of the motherboard. In another aspect of the claim, Pecone does not expressly disclose the riser card operating as a logical extension of the motherboard. Pecone does not expose providing an external interface for the motherboard. Chang et al. teaches a riser card operating as an extension of the motherboard (see Figs. 1-4, "30", "38"; [0023], [0024], [0028]). The riser card (see "30"), as presented by Chang et al. provides an external interface for the motherboard (see [0034]). Chang et al. does not explicitly cite causing a driver to be loaded. However, it does teach a riser card having "plug-in" functionality (see [0001]). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of

the invention to cause a driver to be loaded in order to provide plug and play (PnP) functionality.

As for Claim 20, Pecone includes a riser card coupled with the motherboard via a slot interface having pins corresponding to one or more predetermined standards (see col. 8, lines 13-17; col. 7, lines 34-38; col. 3, lines1-3), as claimed.

As for Claims 22-26, the claimed limitations (audio codec, modem codec, USB support, SMBus device support, and networking functionality) constitute specific examples of possible applications of the memory disclosed by the combination of references, as exposed previously. Therefore, these claims are rejected under the same rationale.

As for Claim 27, Pecone does not explicitly include a sequence of instructions to cause a driver to be loaded based, at least in part, on the one or more indications. It would have been obvious to modify the disclosure in order to include a driver. Chang et al. does not explicitly cite causing a driver to be loaded. Nonetheless, it does teach a riser card having "plug-in" functionality (see [0001]). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention to cause a driver to be loaded in order to provide plug and play (PnP) functionality. It is well known in the art that a driver is code that works to communicate an operating system and a hardware device.

7. Claims 3, 12, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pecone [US 5,604,871] in view of Chang et al. [2001/0014927 A1] in further view of the technical disclosure by IBM (*Enhanced Riser Card with Expansion Function Capability for Personal Computer,* Technical Disclosure Bulletin, July 1994).

As for Claim 3, the combination of references does not specify the memory of the riser card as ROM. A BIOS boot sequence is not disclosed. However, the IBM technical disclosure teaches expanding the functionality of a riser card by including a Basic Input/Output Software (BIOS) and a Read-Only Memory (ROM). It is obvious that this disclosure suggests improving the system disclosed by the combination of references by adding a BIOS and a ROM to the riser card. Accordingly, it would have been obvious to one of ordinary skill in the art to combine the references in order to obtain a low-cost versatile system.

As for Claim 12, the combination of references does not specify the memory of the claimed riser card as ROM or a BIOS boot sequence. However, the IBM disclosure teaches expanding the functionality of a riser card by including a Basic Input/Output Software (BIOS) and a Read-Only Memory (ROM). It is obvious that the disclosure suggests the improvement of the riser card disclosed by the combination of references by adding a BIOS and ROM. Therefore, one of ordinary skill in the art would have been motivated to modify the cited combination of references in order to include the ROM and

BIOS in the riser card, given the benefits in terms of economic factors and upgrading convenience.

As for Claim 21, the combination of references does not specify the memory comprising an interface to couple to a riser card as ROM. However, the technical disclosure by IBM discusses expanding the functionality of a riser card by including a Read-Only Memory (ROM). It is obvious that the IBM disclosure suggests improving the system as disclosed by the combination of references by adding a ROM coupled to the riser card. This improvement would have been obvious given the benefits of the modification in terms of economy and technical upgrading.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Albani et al. [US 5,835,346] discloses a low profile desktop computer.
- Van Rumpt [US 5,594,621] teaches a motherboard for a computer.
- Cobb et al. [US 5,519,573] teaches I/O riser card for motherboard in a personal computer/server.
- Smith [US 5,655,106] teaches personal computer with riser connector for expansion bus and alternate master.
- Horan et al. [US 5,889,970] teaches a system having a core logic chip set configurable for either an accelerated graphics port bus or an additional PCI bus.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel L. Casiano whose telephone number is 703-305-8301. The examiner can normally be reached on 8:00-5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on 703-308-3301. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

alc
November 2, 2003

JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
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